

FEB 22 2007

IN THE CLAIMS

What is claimed is:

1. (Currently Amended) A system on a programmable chip, the system comprising:  
memory;  
a processor coupled to memory, the processor on the programmable chip, the processor  
operable to write streaming output information to memory;  
a streaming output peripheral on the programmable chip configured to generate clock  
cycle accurate output signals, wherein the clock cycle accurate output signals are generated by  
reading streaming output information from memory and outputting signals based on the  
streaming output information.
2. (Currently Amended) The system of claim 1, wherein the memory, processor, and  
streaming output peripheral are connected to a simultaneous multiple primary component fabric,  
the simultaneous multiple primary component fabric allowing a first primary component access  
to a first secondary component at the same time a second primary component is accessing a  
second secondary component.
3. (Original) The system of claim 1, wherein the streaming output information includes  
amplitude and timing information.
4. (Original) The system of claim 1, wherein the streaming output information comprises  
a sequence of values written to memory.
5. (Original) The system of claim 4, wherein the sequence of values is associated with a  
periodic waveform.
6. (Original) The system of claim 4, wherein the sequence of values is associated with an  
event driven waveform.
7. (Original) The system of claim 4, wherein the sequence of values is associated with a  
scripted waveform.
8. (Original) The system of claim 1, wherein the streaming output peripheral operates as  
a streaming parallel output.
9. (Original) The system of claim 1, wherein the streaming output peripheral operates as  
a digital to analog converter (DAC).
10. (Original) The system of claim 1, wherein the streaming output peripheral operates  
as a pulse width modulator (PWM).

11. (Original) The system of claim 1, wherein clock cycle accurate output values are generated during expected clock cycles.

12. (Original) The system of claim 11, wherein clock cycle accurate output values form clock cycle accurate waveforms.

13. (Original) The system of claim 12, wherein the clock cycle accurate waveform is generated without intervention from the processor.

14. (Original) The system of claim 1, wherein the streaming output peripheral receives address information from the processor indicating where to read streaming output information.

15. (Original) The system of claim 14, wherein address information comprises one or more memory addresses.

16. (Original) The system of claim 1, wherein the memory, processor, and streaming output peripheral are connected using a simultaneous multiple primary component fabric.

17. (Currently Amended) A method for generating a waveform, the method comprising: reading streaming output information from memory, the streaming output information written to memory by a processor core on a programmable chip;

generating clock cycle accurate output signals at a streaming output peripheral on the programmable chip, wherein the clock cycle accurate output signals are generated at the streaming output peripheral by reading streaming output information from memory and outputting signals based on the streaming output information.

18. (Currently Amended) The method of claim 17, wherein the memory, processor, and streaming output peripheral are connected to a simultaneous multiple primary component fabric, the simultaneous multiple primary component fabric allowing a first primary component access to a first secondary component at the same time a second primary component is accessing a second secondary component.

19. (Original) The method of claim 17, wherein the streaming output information includes amplitude and timing information.

20. (Original) The method of claim 17, wherein the streaming output information comprises a sequence of values written to memory.

21. (Original) The method of claim 20, wherein the sequence of values is associated with a periodic waveform.

22. (Original) The method of claim 20, wherein the sequence of values is associated with an event driven waveform.

23. (Original) The method of claim 20, wherein the sequence of values is associated with a scripted waveform.

24. (Currently Amended) An apparatus for generating a waveform, the apparatus comprising:

means for reading streaming output information from memory, the streaming output information written to memory by a processor core on a programmable chip;

means for generating clock cycle accurate output signals on the programmable chip, wherein the clock cycle accurate output signals are generated by reading streaming output information from memory and outputting signals based on the streaming output information.

25. (Currently Amended) The apparatus of claim 24, wherein the memory, processor, and streaming output peripheral are connected to a simultaneous multiple primary component fabric, the simultaneous multiple primary component fabric allowing a first primary component access to a first secondary component at the same time a second primary component is accessing a second secondary component.

26. (Original) The method of claim 24, wherein the streaming output information includes amplitude and timing information.

27. (Original) The method of claim 24, wherein the streaming output information comprises a sequence of values written to memory.

28. (Original) The method of claim 27, wherein the sequence of values is associated with a periodic waveform.